**Materials and Device Innovations for Future Low Power Electronics**

**Prof. Ali Javey**

**Electrical Engineering and Computer Sciences, UC Berkeley**

**演講日期:9:50-11:20 am on Friday (6/12)**

**演講地點:台達館B1璟德講堂**

In this talk, I will give an overview of our research program at UC Berkeley on materials and device innovation for future low power electronics. The topics will include monolayer doping (MLD) which was developed by our group as a new doping technology that utilizes self-assembled monolayers of dopant species on semiconductor surfaces followed by thermal annealing. The process has yielded some of the shallowest junctions reported to date, down to ~3 nm in thickness, and is seen as a promising approach for S/D contacts for future Si and III-V transistors. I will also discuss our work on ultrathin body III-V on insulator (XOI) device concept as a platform for integrating high mobility III-V semiconductors on Si for low power electronics. The platform has enabled us to report p- and n-type III-V FETs with some of the highest mobilities reported to-date on Si substrates with a subthreshold swing as low as ~70 mV/decade, approaching the ideal limit of MOSFETs. While our previous XOI work was based on layer transfer process, I will present our recent unpublished work on *direct growth* of single-crystalline III-V’s with lateral scale up to 10’s of µm on amorphous substrates; presenting a major advance in the field of materials growth and processing. Finally, I will discuss our progress towards scaling the body thickness of XOI platform by using layered 2D semiconductors. I will present progress in contact engineering, doping, heterostructures and tunnel transistors using 2D semiconductors.



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